POLISHED FLASH PROCESS WITH METAL GATES AND IMPROVED PLANARITY

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ABSTRACT

An improved method of making a flash memory cell including a substrate having a floating gate of a first thickness includes depositing an insulator on the substrate and over the floating gate. The insulator is preferably a high quality oxide. A portion of the insulator not covering the floating gate has a second thickness which is greater than the first thickness of the floating gate. The method further includes polishing the insulator until the second thickness is substantially equal to the first thickness. Polishing results in a planar floating gate and insulator layer. The method further includes sequentially depositing a dielectric layer and a control gate layer on the planar floating gate and insulator layer and then etching these layers to complete the stacked gate structure of the memory cell.